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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,828	09/22/2005	Ludwig Schwoerer	915-010.021	5792

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EXAMINER
AGHDAM, FRESHTEH N

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,828	SCHWOERER, LUDWIG	
	Examiner	Art Unit	
	FRESHTEH N. AGHDAM	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Richards et al (US 6,289,048).

As to claims 1 and 10-11, Richards teaches a method of and/or apparatus for correcting quadrature error in an analog quadrature demodulator, comprising: splitting an incoming signal in the analog quadrature demodulator into an in-phase branch and a quadrature branch signal (fig. 1, means 102; fig. 2, means 208); and controllably causing the in-phase branch signal and the quadrature branch signal to co-operate with each other via a digital domain (fig. 2, means 218 and 220) correction circuitry so as to correct the quadrature error (fig. 1, means 128; col. 4, lines 63-65). Richards does not expressly teach controllably causing the in-phase branch signal and the quadrature branch signal to co-operate with each other via an analog domain correction circuitry so as to correct the quadrature error. However, one of ordinary skill in the art would recognize that it is a design choice to place the analog to digital converters 218 and 220 after the quadrature error correction stage instead for correcting the 1/Q mismatch in analog domain. Therefore, it would have been obvious to one of ordinary skill in the art

to place the analog to digital converters after the quadrature error correction stage for the reason stated above.

As to claim 2, Richards teaches that one of the in-phase branch and quadrature branch signals is multiplied in a multiplier with a correction signal in order to produce a multiplication result (fig. 1, means 106).

As to claim 3, Richards teaches that the multiplier is one of the following: a mixer and an adjustable amplifier (means 106).

As to claim 4, Richards teaches that the multiplication result is added in an adder (means 108) to the other of the in-phase branch and quadrature branch signals in order to correct the quadratue error.

As to claim 5, Richards teaches that the adding is performed by subtracting the multiplication result and said other of the in-phase branch and quadrature branch signals from each other (means 108; col. 3, lines 31-45).

As to claim 6, Richards teaches that one of the in-phase branch and quadrature branch signals is the quadrature branch signal and said other of the in-phase branch and quadrature branch signals is the in-phase branch signal. Richards does not expressly teach that one of the in-phase branch and quadrature branch signals is the in-phase branch signal and said other of the in-phase branch and quadrature branch signals is the quadrature branch signal. One of ordinary skill in the art would recognize that it is obvious to subtract the scaled version of the in-phase signal instead of subtracting the scaled version (multiplication result) of the quadrature signal from the in-

phase signal (e.g. phase errors can be modeled as a portion of the quadrature branch signal leaking into the in-phase branch signal).

As to claim 7, Richards teaches that said correction signal is a signal relating to the quadrature error (col. 3, lines 32-45).

As to claim 8, Richards teaches correction signal is a signal that is between -1 and 1 (col. 7, lines 12-22). One of ordinary skill in the art would recognize that the correction signal as taught by Richards is proportional to sinε since sin ε has a value between -1 and 1, therefore, the correction signal C1 as taught by Richards could be shown in terms of sinε.

As to claim 9, Richards further teaches generating said correction signal based on a cross correlation calculation of the digital domain in-phase branch and quadrature branch signals; and feeding back the correction signal generated correction circuitry (means 126 and 128). Richards does not expressly teach converting the analog in-phase branch and quadrature branch signals to digital after the quadrature error correction stage. However, one of ordinary skill in the art would recognize that it is a design choice to place the analog to digital converters 218 and 220 after the quadrature error correction stage instead for correcting the 1/Q mismatch in analog domain. Therefore, it would have been obvious to one of ordinary skill in the art to place the analog to digital converters after the quadrature error correction stage for the reason stated above.

As to claims 12-15, one of ordinary skill in the art would recognize that the I/Q mismatch correction is utilized in the receiver of a communication system that employs

a type of quadrature modulation scheme in order to compensate for the phase and gain mismatches, wherein the communication system would be an OFDM system or DVB-T, and also, the I/Q mismatch correction would be utilized in a cellular network such as a cellular telephone network or could be utilized in a mobile station in order to suppress these errors and enhance the system performance.

As to claim 16, Richards teaches forcing the quadrature error towards zero by using a correction loop (fig. 1 and 3, means 320) such as an integrator loop or proportional integrator loop (e.g. summer, col. 6, lines 35-39).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Genrich (US 6,661,852) see figure 5.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRESHTEH N. AGHDAM whose telephone number is (571)272-6037. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Freshteh N Aghdam/

Examiner, Art Unit 2611

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611